

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
Memory Access Operations (continued)									
LDBSE	2	D \leftarrow A D+1 \leftarrow Sign(A)	—	—	—	—	—	—	3,4
	2	D \leftarrow A D+1 \leftarrow 0	—	—	—	—	—	—	3,4
PUSH	1	SP \leftarrow SP-2 (SP) \leftarrow A	—	—	—	—	—	—	
	1	A \leftarrow (SP) SP \leftarrow SP+2	—	—	—	—	—	—	
POPF	0	SP \leftarrow SP-2 (SP) \leftarrow PSW PSW \leftarrow 0000H I \leftarrow 0	0	0	0	0	0	0	
	0	PSW \leftarrow (SP) SP \leftarrow SP+2 I \leftarrow $\sqrt{ }$	✓	✓	✓	✓	✓	✓	
Control Flow Operations									
SJMP	1	PC \leftarrow PC + 11-bit offset	—	—	—	—	—	—	5
LJMP	1	PC \leftarrow PC + 16-bit offset	—	—	—	—	—	—	5
BR(indirect)	1	PC \leftarrow (A)	—	—	—	—	—	—	
SCALL	1	SP \leftarrow SP-2 (SP) \leftarrow PC PC \leftarrow PC + 11-bit offset	—	—	—	—	—	—	5
	1	SP \leftarrow SP-2 (SP) \leftarrow PC PC \leftarrow PC + 16-bit offset	—	—	—	—	—	—	5
RETF	0	PC \leftarrow (SP) SP \leftarrow SP+2	—	—	—	—	—	—	
J(condition)	1	PC \leftarrow PC + 8-bit offset (if taken)	—	—	—	—	—	—	5
JC	1	Jump if C = 1	—	—	—	—	—	—	5
JNC	1	Jump if C = 0	—	—	—	—	—	—	5
JE	1	Jump if Z = 1	—	—	—	—	—	—	5
JNE	1	Jump if Z = 0	—	—	—	—	—	—	5
JGE	1	Jump if N = 0	—	—	—	—	—	—	5
JLT	1	Jump if N = 1	—	—	—	—	—	—	5
JGT	1	Jump if N = 0 and Z = 0	—	—	—	—	—	—	5
JLE	1	Jump if N = 1 or Z = 1	—	—	—	—	—	—	5
JH	1	Jump if C = 1 and Z = 0	—	—	—	—	—	—	5
JNH	1	Jump if C = 0 or Z = 1	—	—	—	—	—	—	5
JV	1	Jump if V = 1	—	—	—	—	—	—	5
JNV	1	Jump if V = 0	—	—	—	—	—	—	5
JVT	1	Jump if VT = 1 Clear VT	—	—	—	—	—	—	5
	1	Jump if VT = 0 Clear VT	—	—	—	—	—	—	5

Mnemonic	Operands	Operation (Note 1)	Flags						Notes
			Z	N	C	V	VT	ST	
Control Flow Operations (continued)									
JST	1	Jump if ST = 1	—	—	—	—	—	—	5
JNST	1	Jump if ST = 0	—	—	—	—	—	—	5
JBS	1	Jump if Specified Bit = 1	—	—	—	—	—	—	5,6
JBC	1	Jump if Specified Bit = 0	—	—	—	—	—	—	5,6
DJNZ	1	D ← D - 1 if D ≠ 0 then PC ← PC + 8-bit offset	—	—	—	—	—	—	5
Miscellaneous Operations									
RST	0	PC ← 2080H	0	0	0	0	0	0	8
DI	0	Disable All Interrupts (I ← 0)	—	—	—	—	—	—	
EI	0	Enable All Interrupts (I ← 1)	—	—	—	—	—	—	
NOP	0	PC ← PC + 1	—	—	—	—	—	—	
SKIP	0	PC ← PC + 2	—	—	—	—	—	—	
NORML	2	Left Shift Until msb = 1 D ← shift count	✓	?	0	—	—	—	7
TRAP	0	SP ← SP - 2 (SP) ← PC PC ← (2010H)	—	—	—	—	—	—	9

Flag Operations:

- 1 Always set by operation ✓ Determined by result of operation
- 0 Always cleared by operation ↑ May be set by operation
- ? Undefined after operation ↓ May be cleared by operation
- Unchanged

Notes

1. If the mnemonic ends in "B", a byte operation is performed, otherwise a word operation is done. Operands D, B, and A must conform to the alignment rules for the required operand type. D and B are locations in the register file; A can be located anywhere in memory.
2. D, D + 2 are consecutive WORDS in memory; D is DOUBLE-WORD aligned.
3. D, D + 1 are consecutive BYTES in memory; D is WORD aligned.
4. Changes a byte to a word.
5. Offset is a 2's complement number.
6. Specified bit is one of the 2048 bits in the register file.
7. The "L" (Long) suffix indicates double-word operation.
8. Initiates a Reset by pulling RESET low. Software should re-initialize all the necessary registers with code starting at 2080H.
9. The assembler will not accept this mnemonic.