

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 14.5V
- 3.5Vpp analog signal capability
- R_{ON} 65 Ω max. @ V_{DD} =14V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD} =14V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology

Applications

- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Ordering Information

MT093AE	40 Pin Plastic DIP
MT093AP	44 Pin PLCC

0° to 70°C

Description

The Zarlink MT093 is fabricated in Zarlink's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8x12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven input bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.

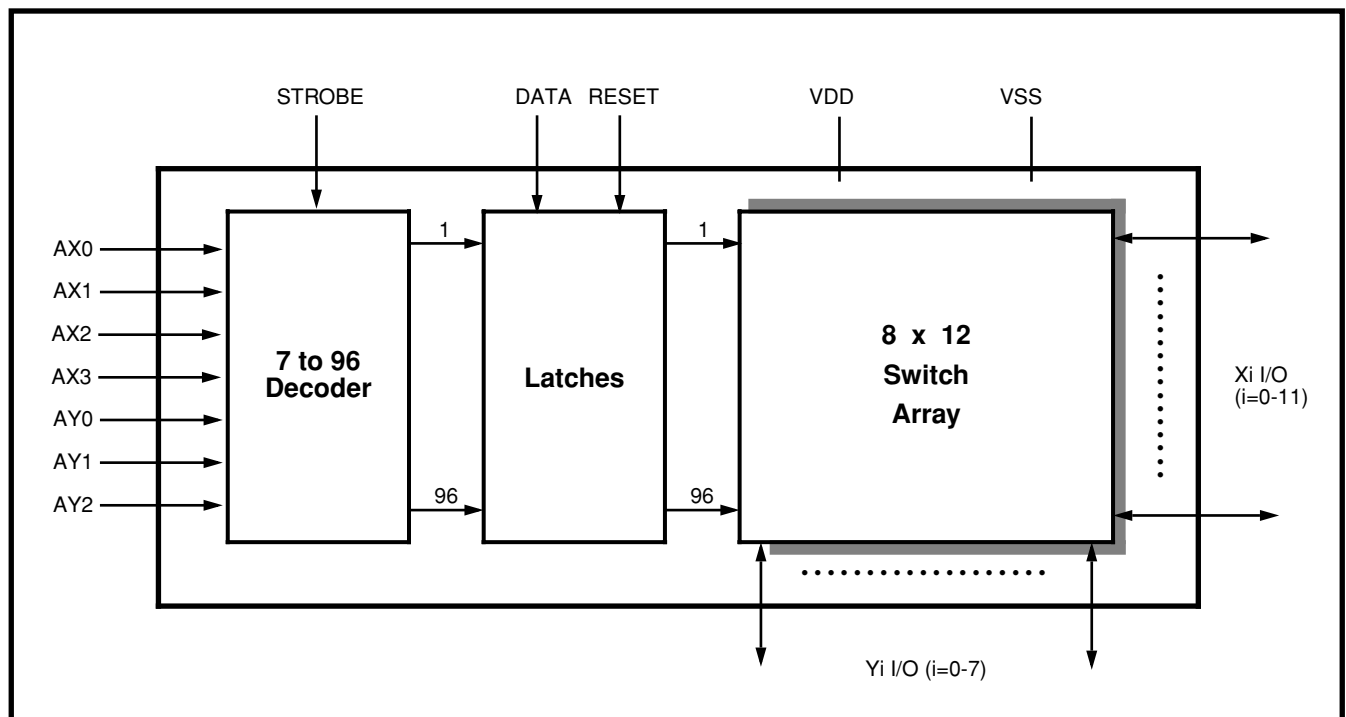


Figure 1 - Functional Block Diagram

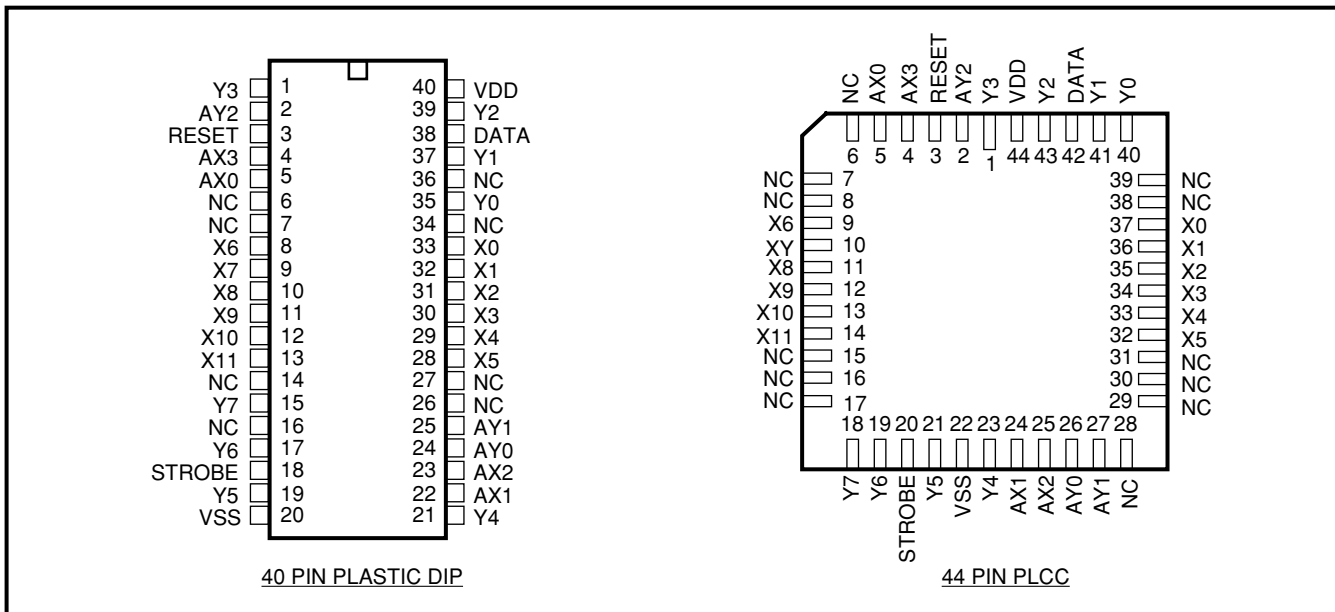


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
PDIP	PLCC		
1	1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array.
2	2	AY2	Y2 Address Line (Input).
3	3	RESET	Master RESET (Input): this is used to turn off all switches. Active High.
4,5	4,5	AX3,AX0	X3 and X0 Address Lines (Inputs).
6,7	6-8	NC	No Connection.
8-13	9-14	X6-X11	X6-X11 Analog (Inputs/Outputs): these are connected to the X6-X11 rows of the switch array.
14	15-17	NC	No Connection.
15	18	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array.
16	-	NC	No Connection.
17	19	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array.
18	20	STROBE	STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	21	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array.
20	22	V _{SS}	Ground Reference.
21	23	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array.
22, 23	24,25	AX1,AX2	X1 and X2 Address Lines (Inputs).
24, 25	26,27	AY0,AY1	Y0 and Y1 Address Lines (Inputs).
26, 27	28-31	NC	No Connection.
28 - 33	32-37	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array.
34	38,39	NC	No Connection.
35	40	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array.
36	-	NC	No Connection.
37	41	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array.

Pin Description

Pin #		Name	Description
PDIP	PLCC		
38	42	DATA	DATA (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	43	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array.
40	44	V _{DD}	Positive Power Supply.

Functional Description

The MT093 is an analog switch matrix with an array size of 8 x 12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y input/output lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address input lines (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input line. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input line will asynchronously return all memory locations to logical "0" turning off all crosspoint switches.

Address Decode

The seven address lines along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	16.0	V
		V_{SS}	-0.3	$V_{DD}+0.3$	V
2	Analog Input Voltage	V_{INA}	-0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage	V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin	I		±15	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP	P_D	0.6	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	0	25	70	°C	
2	Supply Voltage	V_{DD}	4.5		14.5	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		3.5	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{SS}=0V$, $V_{DD}=14V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DDQ}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				7	15	mA	All digital inputs at $V_{IN}=2.4V$
2	Off-state Leakage Current	I_{OFF}			±1	μA	$ V_{Xi} - V_{Yj} = V_{DD} - V_{SS}$
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V_{IH}	2.4			V	
5	Input Leakage (digital pins)	I_{LEAK}			10	μA	All digital inputs at $V_{IN} = V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{IDC}/V_{ODC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		60°C		70°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance $V_{DD}=14V$	R_{ON}	45	65				75	Ω	$V_{SS}=0V$, $ V_{Xi}-V_{Yj} = 0.25V$ $V_{IDC}=6.75V$ $V_{ODC}=6.5V$
2	Difference in on-state resistance between two switches	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=14V$, $V_{SS}=0$, $V_{IDC}=6.75V$ $V_{ODC}=6.5V$ $ V_{Xi}-V_{Yj} = 0.25V$

AC Electrical Characteristics† - Crosspoint Performance - V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to $V_{DD}=7V$, $V_{DC}=0V$, $V_{SS}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	$f=1$ MHz
2	Feedthrough Capacitance	C_F		0.2		pF	$f=1$ MHz
3	Frequency Response Channel "ON" $20\text{LOG}(V_{OUT}/V_{Xi})=-3\text{dB}$	$F_{3\text{dB}}$		45		MHz	Switch is "ON"; $V_{INA} = 2\text{Vpp}$ sinewave; $R_L = 1\text{k}\Omega$
4	Total Harmonic Distortion	THD		0.05		%	Switch is "ON"; $V_{INA} = 2\text{Vpp}$ sinewave $f= 1\text{kHz}$; $R_L=1\text{k}\Omega$
5	Feedthrough Channel "OFF" Feed.= $20\text{LOG}(V_{OUT}/V_{Xi})$	FDT		-95		dB	All Switches "OFF"; $V_{INA}= 2\text{Vpp}$ sinewave $f= 1\text{kHz}$; $R_L= 1\text{k}\Omega$.
6	Crosstalk between any two channels for switches X_i - Y_i and X_j - Y_j . $X_{\text{talk}}=20\text{LOG}(V_{Yj}/V_{Xi})$.	X_{talk}		-45		dB	$V_{INA}=2\text{Vpp}$ sinewave $f= 10\text{MHz}$; $R_L = 75\Omega$.
				-90		dB	$V_{INA}=2\text{Vpp}$ sinewave $f= 10\text{kHz}$; $R_L = 600\Omega$.
				-85		dB	$V_{INA}=2\text{Vpp}$ sinewave $f= 10\text{kHz}$; $R_L = 1\text{k}\Omega$.
				-80		dB	$V_{INA}=2\text{Vpp}$ sinewave $f= 1\text{kHz}$; $R_L = 10\text{k}\Omega$.
7	Propagation delay through switch	t_{PS}			50	ns	$R_L=1\text{k}\Omega$; $C_L=50\text{pF}$

† Timing is over recommended temperature range.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Crosstalk measurements are for Plastic DIPs only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings - V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to $V_{DD}=7V$, $V_{DC}=0V$, $V_{SS}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		50		mVpp	$V_{IN}=3V+V_{DC}$ squarewave; $R_{IN}=1\text{k}\Omega$, $R_L=10\text{k}\Omega$.
2	Digital Input Capacitance	C_{DI}		10		pF	$f=1\text{MHz}$
3	Switching Frequency	F_O			10	MHz	
4	Setup Time DATA to STROBE	t_{DS}	20			ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
5	Hold Time DATA to STROBE	t_{DH}	20			ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
6	Setup Time Address to STROBE	t_{AS}	20			ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
7	Hold Time Address to STROBE	t_{AH}	20			ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
8	STROBE Pulse Width	t_{SPW}	40			ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
9	RESET Pulse Width	t_{RPW}	80			ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
10	STROBE to Switch Status Delay	t_S		80	200	ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
11	DATA to Switch Status Delay	t_D		100	200	ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$
12	RESET to Switch Status Delay	t_R		70	200	ns	$R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$

† Timing is over recommended temperature range.

Digital Input rise time (t_r) and fall time (t_f) = 10ns.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

*

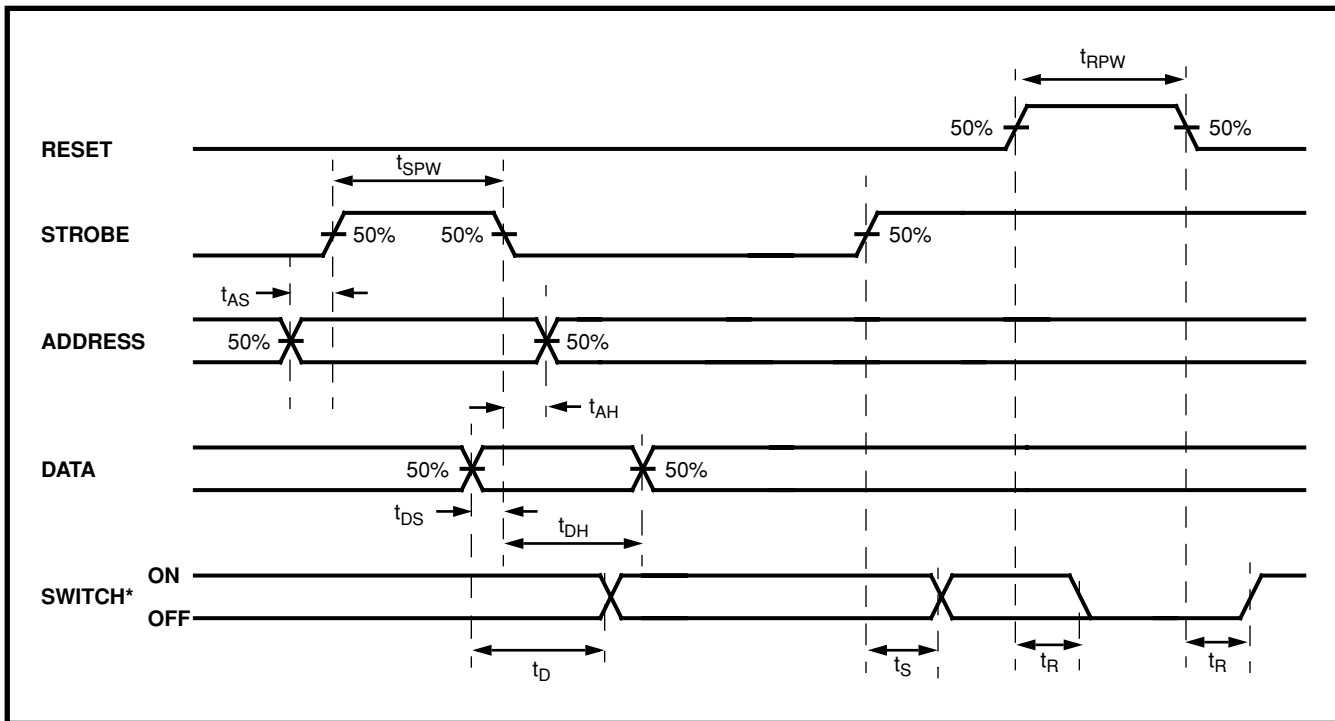
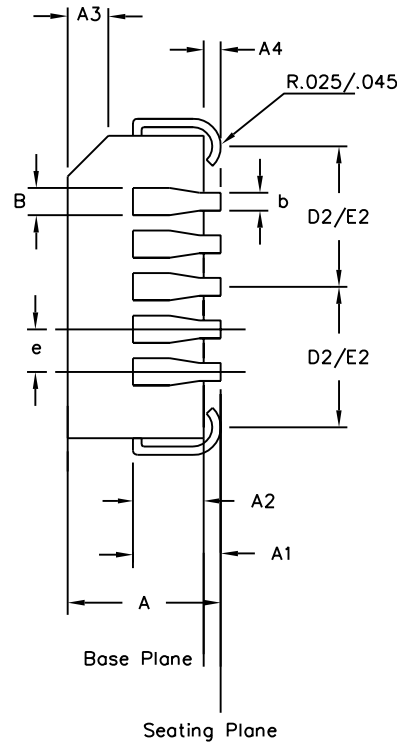
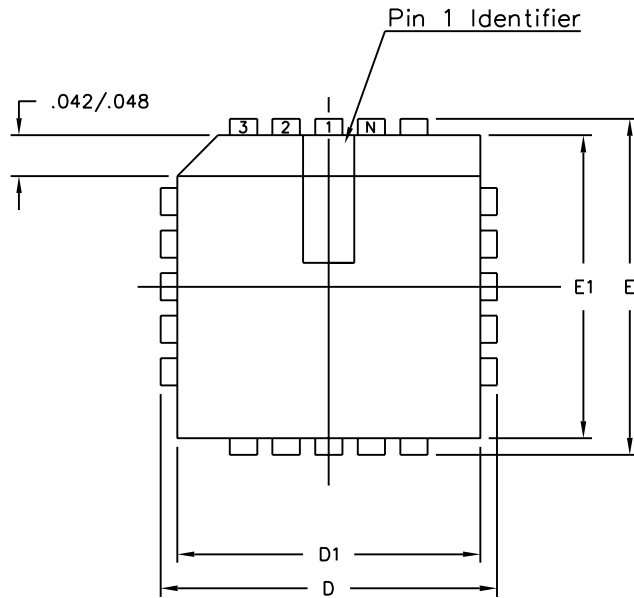


Figure 3 - Control Memory Timing Diagram

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection ^①
1	1	1	0	0	0	0	No Connection ^①
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection ^①
1	1	1	1	0	0	0	No Connection ^①
0	0	0	0	1	0	0	X0-Y1
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	0	0	X11-Y1
0	0	0	0	0	1	0	X0-Y2
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	1	0	X11-Y2
0	0	0	0	1	1	0	X0-Y3
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	1	0	X11-Y3
0	0	0	0	0	0	1	X0-Y4
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	0	1	X11-Y4
0	0	0	0	1	0	1	X0-Y5
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	0	1	X11-Y5
0	0	0	0	0	1	1	X0-Y6
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	0	1	1	X11-Y6
0	0	0	0	1	1	1	X0-Y7
↓	↓	↓	↓	↓	↓	↓	↓
1	0	1	1	1	1	1	X11-Y7

Table 1. Address Decode Truth Table

^① This address has no effect on device status.



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	—	0.51	—
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050	BSC	1.27	BSC
Pin features				
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

© Zarlink Semiconductor 2002 All rights reserved.

ISSUE	1	2	3
ACN	5958	207470	213094
DATE	15Aug94	10Sep99	15Jul02
APPRD.			



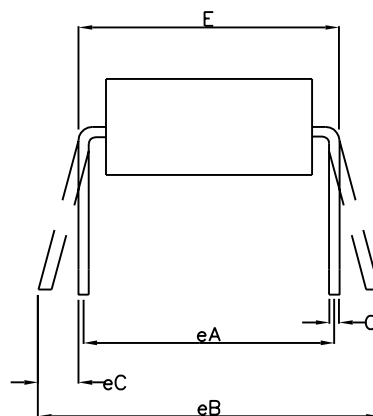
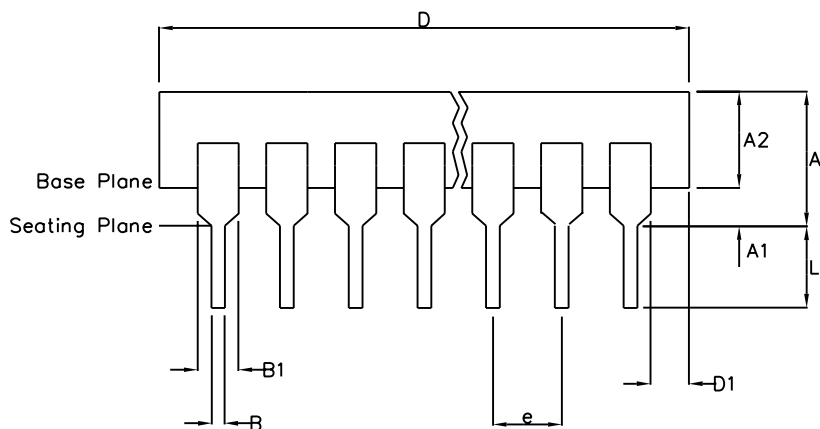
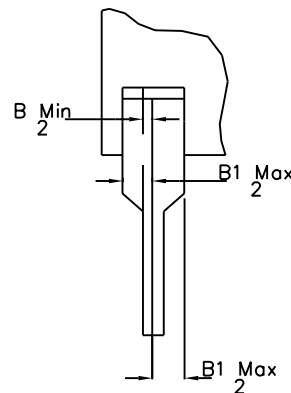
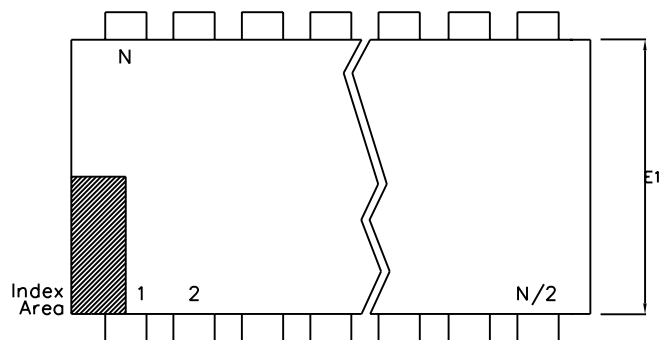
Previous package codes

HP / P

Package Code QA

Package Outline for
44 lead PLCC

GPD00003



	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jeduc MS-011AC ISS.B				

Notes:

1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

© Zarlink Semiconductor 2002 All rights reserved.

ISSUE	1	2	3
ACN	7010	203533	213103
DATE	20Apr95	25Nov97	15Jul02
APPRD.			



Previous package codes

DP / E

Package Code DA

Package Outline for
40 lead PDIP

GPD00073



**For more information about all Zarlink products
visit our Web Site at
www.zarlink.com**

Information relating to products and services furnished herein by Zarlink Semiconductor Inc. or its subsidiaries (collectively "Zarlink") is believed to be reliable. However, Zarlink assumes no liability for errors that may appear in this publication, or for liability otherwise arising from the application or use of any such information, product or service or for any infringement of patents or other intellectual property rights owned by third parties which may result from such application or use. Neither the supply of such information or purchase of product or service conveys any license, either express or implied, under patents or other intellectual property rights owned by Zarlink or licensed from third parties by Zarlink, whatsoever. Purchasers of products are also hereby notified that the use of product in certain ways or in combination with Zarlink, or non-Zarlink furnished goods or services may infringe patents or other intellectual property rights owned by Zarlink.

This publication is issued to provide information only and (unless agreed by Zarlink in writing) may not be used, applied or reproduced for any purpose nor form part of any order or contract nor to be regarded as a representation relating to the products or services concerned. The products, their specifications, services and other information appearing in this publication are subject to change by Zarlink without notice. No warranty or guarantee express or implied is made regarding the capability, performance or suitability of any product or service. Information concerning possible methods of use is provided as a guide only and does not constitute any guarantee that such methods of use will be satisfactory in a specific piece of equipment. It is the user's responsibility to fully determine the performance and suitability of any equipment using such information and to ensure that any publication or data used is up to date and has not been superseded. Manufacturing does not necessarily include testing of all functions or parameters. These products are not suitable for use in any medical products whose failure to perform may result in significant injury or death to the user. All products and materials are sold and services provided subject to Zarlink's conditions of sale which are available on request.

Purchase of Zarlink's I²C components conveys a licence under the Philips I²C Patent rights to use these components in and I²C System, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Zarlink, ZL and the Zarlink Semiconductor logo are trademarks of Zarlink Semiconductor Inc.

Copyright Zarlink Semiconductor Inc. All Rights Reserved.

TECHNICAL DOCUMENTATION - NOT FOR RESALE
